MEng Project: Chip-Scale Atomic Clock

Time: 14:00Hrs Location: 4East EEE lab

Members: AA, QG, BD, JT, NR, JS, YL

Meeting notes:

* PMG meeting – 14:15 – meet & greet session
* AA Risk mitigation measure – attend the PMG meeting with Ben.
* Work out what design strategy
* Request guidance on sales, marketing research and strategy
* Ben Draper: Methods to ensure coverage on standards, and legal issues on electronics.
* Needs analysis –Needs ranking
* Chronos technology: chase scope exercise (Abba)
* Risk assessment and analysis
* Prof. Mitchell. – Address team questions relating to clocks, Project Scope ?
* Ranking with criteria, based on competitors, and market research
* Atomic clock for measuring units/timing sensors work perfectly/why would we need to increase the precision of synchronization between the units?
* Define benchmark comparison parameters/variables
* Nikola to investigate resource & expertise from Dr Clarke in FPGA Clock Verilog Implementation (Extra-high precision), Microelectronics with clocks and dealing with jitter
* Nikola + Abba went to SSTL presentation to aid relationship building & expertise access
* Prototyping stage pursues product development after feasibility report.
* Post-feasibility report shall lead into design specification of the prototype.
* Need a functional specification analysis.

Summary

1. Ask Prof. Mitchell about coverage legal standards for GPS, and technical devices
2. Marketing and Business strategy conduct research on what product is needed to do to fit the standards